STATUS OF THE APPLICATION

- Claims 1-8 and 11-20 are rejected under 35 U.S.C. § 102(a), (e) as being anticipated by U.S. Patent No. 6,617,621 to *Gheewala et al.* ("*Gheewala*").
- Claims 9-10 are rejected under 35 U.S.C. § 103(a) as being obvious over *Gheewala*.
- Claim 13 is objected to on the basis of informalities.

REMARKS

General

Please cancel claims 6-8.

The Objection to Claim 13

As requested by the Examiner, claim 13 has been corrected so as to remove the identified objectionable language.

The Rejections under 35 U.S.C. § 102(a), (e)

Claims 1-5 and 11-20 have been rejected under 35 U.S.C. § 102(a) and/or (e) as being unpatentable over *Gheewala*. Applicants respectfully traverse, noting that *Gheewala* does not disclose all elements of claims 1-5 and 11-20 as amended. More specifically, *Gheewala* only discloses standard pre-fabrication of individual ICs, which are known to have IP integration and floor planning requirements. It does not disclose wafers having multiple dice that can each be programmed into a different concept-validating IC, nor does it disclose a process flow for fabricating separate ICs from each of these concept-validating ICs without IP integration or floor planning requirements.

Gheewala discloses standard device pre-fabrication. The first three metal layers (M1 – M3) of an IC are pre-fabricated, allowing the next two metal layers (M4 – M5) to be custom designed so as to custom-interconnect these prefabricated gates (Col. 10:29-41).

Initially, note that *Gheewala* only discloses pre-fabrication of individual ICs – its drawings all show device-level components of a single IC, and its description does not extend to the wafer level. In contrast, Applicants' claims 1 and 11 recite a wafer having a plurality of dice, each "configured to be separately programmed into a customized concept validating IC."

Furthermore, even if *Gheewala* can be extended to the wafer level, *Gheewala* does not disclose wafers with different concept validating (i.e., "proof-of-concept") ICs on them, nor does it disclose design flows for fabricating separate ICs from each different concept validating IC with no intellectual property (IP) integration or floor planning requirements. As noted in Applicants' specification as filed, prior art pre-fabricated circuits, such as those used by *Gheewala*, have separate sets of IP, as well as separate floor planning requirements, for each

different IC (Specification, ¶¶ 9, 63). A wafer with multiple different ICs would thus require integration of these different IP sets and floor planning requirements before it could be produced. In contrast, the required IP is already integrated into Applicants' SMPWs (Specification, ¶¶ 63), and the floor planning requirement for each IC is already known, as it is pre-fabricated up to the contact level (Id.) Claims 1 and 11 thus disclose design flows for fabricating separate ICs, with "no IP integration or floor planning requirements." Accordingly, claims 1 and 11 are patentable over *Gheewala* for at least this reason. Similarly, claims 2-5, and 12-20 depend from claims 1 and 8 respectively, and are thus patentable over *Gheewala* for at least this same reason.

The Rejections under 35 U.S.C. § 103(a)

Claims 9-10 are rejected under 35 U.S.C. § 103(a) as being obvious over *Gheewala*. For the same reasons as described above, Applicants respectfully traverse, noting that Gheewala does not disclose all elements of claims 9-10 as amended. More specifically, *Gheewala* does not disclose wafers with multiple dice, "each die configured to be separately programmed into a customized concept validating IC" nor does it disclose design flows for fabricating separate ICs, with "no IP integration or floor planning requirements."

CONCLUSION

In view of the above, it is respectfully submitted that Claims 1-5 and 9-20 are now in condition for allowance.

The Examiner is invited to call Applicants' attorney at the number below in order to speed the prosecution of this application.

The Commissioner is authorized to charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 07-1896.

Respectfully submitted,

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